Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each.

1   1. (Previously Presented) A data processing device including:

2   a processor;

3   a charge storage device coupled to the processor;

4   a current source for supplying the processor with substantially constant

5   operating current at multiple nonzero current levels, and adapted to vary its

6   output current independently of an instantaneous power demand of the

7   processor by switching either periodically or aperiodically between the multiple

8   nonzero current levels.

1   2. (Currently Amended) The device of claim 1 <u>wherein</u> ~~in which~~ the charge

2   storage device comprises a capacitor in series with the current source, and

3   across which the processor is connected in parallel.

1   3. (Currently Amended) The device of claim 1 <u>wherein</u> ~~in which~~ the current

2   source is adapted to periodically or aperiodically switch between two different

3   nonzero current levels.

4. (Canceled)

1   5. (Currently Amended) The device of claim 3 <u>wherein</u> ~~in which~~ the <u>current</u>

2   <u>source determines the</u> interval between switching current levels <u>based on</u> ~~is~~

3   ~~determined by~~ an average power demand of the processor.

1   6. (Currently Amended) The device of claim 1 <u>wherein</u> ~~in which~~ the current

2   source further comprises:

3   a second current source adapted to provide a noise current that varies on

4   a random or pseudo-random basis.

1   7. (Currently Amended) The device of claim 1 further including <u>a </u>control means

2   <u>for the current source</u> ~~adapted~~ to maintain the supply voltage to the processor

3   between an upper voltage limit and a lower voltage limit.

1   8. (Currently Amended) The device of claim 1 further including a zener diode

2   ~~adapted~~ to maintain the supply voltage to the processor between an upper

3   voltage limit and a lower voltage limit.

1   9. (Currently Amended) The device of claim 7 <u>wherein</u> ~~in which~~ the control

2   means includes <u>a</u> current switching means for switching the current source

3   between a first, higher current level and a second, lower current level, the

4   current level switching being triggered by the supply voltage to the processor

5   respectively reaching the lower voltage limit and the upper voltage limit.

1   10. (Original) The device of claim 9 further including a timer for determining a

2   time period taken for the processor supply voltage to reach a lower voltage limit

3   from an upper voltage limit, or vice versa.

1   11. (Currently Amended) The device of claim 10 further including current

2   setting means for varying at least one from among the first current level and

3   and/or the second current level of the current source if the timer determines

4   that the time period falls outside the predetermined limits.

1   12. (Currently Amended) The device of claim 11 wherein the predetermined

2   limits include a first predetermined threshold, and wherein in which the

3   current setting means raises the first current level if the timer determines that

4   the time period for reaching the lower voltage limit falls below the [[a]] first

5   predetermined threshold.

1   13. (Currently Amended) The device of claim 11 wherein the predetermined

2   limits include a second predetermined threshold, and wherein in which the

3   current setting means reduces the first current level if the timer determines

4   that the time period for reaching the lower voltage limit exceeds the [[a]] second

5   predetermined level.

1   14. (Currently Amended) The device of claim 11 wherein the predetermined

2   limits include a first predetermined threshold, and wherein in which the

3   current setting means reduces the second current level if the timer determines

4   that the time period for reaching the upper voltage limit exceeds the [[a]] first

5   predetermined level.

1   15. (Currently Amended) The device of claim 11 wherein the predetermined

2   limits include a second predetermined threshold, and wherein in which the

3   current setting means raises the second current level if the timer determines

4   that the time period for reaching the upper voltage limit exceeds the [[a]] second

5   predetermined level.

1   16. (Currently Amended) The device of claim 9 wherein in which the control

2   means includes means for temporarily inhibiting the current switching means if

3   the supply voltage to the processor fails to move towards the desired upper

4   voltage limit or the lower voltage limit.

1   17. (Currently Amended) The device of claim 1 wherein in which the processor

2   has an internal clock having a ,the frequency that of which is dependent upon

3   the supply voltage to the processor.

1   18. (Currently Amended) The device of claim 1 wherein in which the processor

2   is a cryptographic processor.

1   19. (Currently Amended) The device of claim 1 further comprising a

2   incorporated into a smart card supporting the processor, the charge storage

3   device, and the current source.

1   20. (Currently Amended) A method of operating a data processing device

2   comprising the steps of:

3   drawing current from the an external power supply; and

4   utilizing the drawn current, [[to]] generating and cyclically apportioning

5   a substantially constant current flow from a current source between a charge

6   storage device and a processor within the data processing device,

7   wherein the substantially constant current flow that is periodically or

8   aperiodically switched between multiple different nonzero current levels, such

9   that the drawn current varies independently of the instantaneous power

10   demand of the processor.

1   21. (Currently Amended) The method of claim 20 wherein further including the

2   step of utilizing the drawn current for generating and apportioning generate a

3   current flow to the processor and the charge storage device switches, that is

4   periodically or aperiodically, switched between two different nonzero current

5   levels.

     22. (Canceled)

1   23. (Currently Amended) The method of claim 21 wherein further including the

2   step of generating and apportioning a current flow includes determining the

3   interval between switching according to an average power demand of the

4   processor.

1   24. (Currently Amended) The method of claim 20 <u>wherein the step of generating</u>

2   <u>and apportioning a current flow utilizes a first current source, and</u> further

3   <u>includes</u> ~~including the steps of~~:

4   utilizing a second current source to provide a superposed current that

5   varies on a random or pseudorandom basis and

6   delivering the combined current of the first and second current sources to

7   the processor and the charge storage device.

1   25. (Previously Presented) The method of any one of the claims 20, 21, 23, and

2   24 further including the step of maintaining a supply voltage to the processor

3   between an upper voltage limit and a lower voltage limit.

1   26. (Currently Amended) The method of claim 25 <u>wherein</u> ~~further including~~ the

2   step of <u>generating and apportioning a current flow switches the</u> ~~switching a~~

3   current source between a first, higher current level and a second, lower, current

4   level, when the supply voltage to the processor respectively reaches the lower

5   voltage limit and the higher voltage limit.

1   27. (Currently Amended) The method of claim 26 <u>wherein the step of generating</u>

2   <u>and cyclically apportioning a current flow</u> further <u>includes</u> ~~including~~ the steps

3   of:

4   determining a time period taken for the processor supply voltage to reach

5   a lower voltage limit from an upper voltage limit, or vice versa, and

6   varying the first current level and/or the second current level of the

7   current source if the time period falls outside predetermined limits.

1   28. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ raising the first current level if the time

3   period for reaching the lower voltage limit falls below a first predetermined

4   threshold.

1   29. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ reducing the first current level if the time

3   period for reaching the lower voltage limit exceeds a second predetermined

4   threshold.

1   30. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ reducing the second current level of the

3   time period for reaching the upper voltage limit falls below a first

4   predetermined threshold.

1   31. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ raising the second current level if the time

3   period for reaching the upper voltage limit exceeds a second predetermined

4   threshold.

1   32. (Currently Amended) The method of claim 26 further including the step of

2   temporarily inhibiting the current switching if the supply voltage to the

3   processor fails to move towards the ~~desired~~ upper <u>voltage limit</u> or <u>the</u> lower

4   voltage limit.

1   33. (Original) The method of claim 20 further including the step of controlling

2   the frequency of operation of the processor as a function of the supply voltage to

3   the processor.

34-35. (Canceled)

1   36. (Currently Amended) The method of claim 28 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ reducing the first current level if the time

3   period for reaching the lower voltage limit exceeds a second predetermined

4   threshold.